

In the Claims:

1. (previously presented) A process of selecting different 1149.1 TAP domain arrangements within an integrated circuit comprising:

A. performing an 1149.1 instruction shift operation through a first 1149.1 TAP domain arrangement;

B. performing an 1149.1 instruction update operation at the end of the 1149.1 instruction shift operation; and

C. in response to said 1149.1 instruction update operation, selecting a second 1149.1 TAP domain arrangement that differs from the first 1149.1 TAP domain arrangement.

2. (cancelled)

3. (previously presented) The process of claim 1 including performing the 1149.1 instruction shift operation in accordance with the 1149.1 IEEE Standard titled Test Access Port and Boundary-Scan Architecture.

4. (previously presented) The process of claim 1 including performing the 1149.1 instruction update operation in accordance with the 1149.1 IEEE Standard titled Test Access Port and Boundary-Scan Architecture.

5. (previously presented) The process of claim 1 including performing a select DR operation, a select IR operation, and a capture IR operation before performing the instruction shift operation.

6. (previously presented) The process of claim 1 including performing one of a select DR operation and a Run Test/Idle operation after performing the instruction update operation.